ABSTRACT OF THE DISCLOSURE

A digital multilevel signal receiver circuit which can sufficiently improve transmission efficiency while suppressing a data transmission error, and an automatic equalization circuit for use in the digital multilevel signal receiver circuit. An equalization training automatic equalizer is provided separately from a data reproducing equalizer having equalization characteristics which can be set up. A received training signal is once stored in a memory, read out from the memory and supplied to the equalization training automatic equalizer so as to update tap coefficients of the equalizer. The updated tap coefficients are given to the data reproducing equalizer so as to update equalization characteristics of the equalizer. A received data signal is equalized with the updated equalization characteristics.